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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/352,959	07/14/1999	PAUL W. CAMPBELL	0100.9900940	2833

23418 7590 04/07/2004

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EXAMINER	
VITAL, PIERRE M	
ART UNIT	PAPER NUMBER
2188	16

DATE MAILED: 04/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/352,959	CAMPBELL, PAUL W.	
	Examiner	Art Unit	
	Pierre M. Vital	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,6-12 and 17-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1,6,12 and 17* is/are allowed.

6)☒ Claim(s) *7-12 and 18-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 July 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on March 12, 2004 has been entered.

Response to Amendment

2. This Office Action is in response to applicant's communication filed March 12, 2004 in response to PTO Office Action mailed February 25, 2004. The Applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

3. Claims 1, 6-12 and 17-22 have been presented for examination in this application. In response to the last Office Action, claims 1 and 12 have been amended. No claims have been canceled or added. As a result, claims 1, 6-12 and 17-22 are now pending in this application.

4. The rejection of claims 7-11 and 18-22 as in the Office Action mailed July 18, 2003 (Paper No. 9) is respectfully maintained and reiterated below for applicant's convenience.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 7 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakatsuka et al (US6,433,782) and Bogin et al. (US6,192,455).

As per claims 7 and 18, Nakatsuka discloses a processing module [abstract, line 2]; and memory operably coupled to the processing module, wherein the memory stores operational instructions that cause the processing module to [abstract, lines 2-3]; (a) translate a virtual address into an address [*logical address translated to physical address*; col. 9, lines 5-8]; (b) determine whether the address corresponds to translation memory space [*determining which regions the data accessed by the processor belongs*; col. 9, lines 13-16]; (d) translate the address into another address when the address corresponds to translation memory space; (e) caching the another address in the translation look aside [*logical address is converted to physical address corresponding to graphics address by address converter unit*; col. 8, line 66 – col. 9, line 39].

However, Nakatsuka does not specifically teach translating a virtual address into an address and caching the address and the another address in a translation look aside table when the address corresponds to the translation memory space as recited in the claims.

Bogin discloses translating a virtual address into an address [*translation table 143 has virtual to main memory address translation*; col. 2, lines 46-49; col. 4, lines 5-8] and caching the address [*GTLB 141 is a cache buffer of translation table 143*; col. 4, lines 46-51]; and also caching another address in the same translation look aside table when the address corresponds to the translation memory space [*AGP maps into physical address of main memory 145 which maps into physical address space of system memory 132*; col. 4, lines 2-8; *GTLB 141 has address references from the AGP memory 127 to a corresponding address in main memory 145 of system memory 132;* col. 4, lines 46-51].

It would have been obvious to one of ordinary skill in the art, having the teachings of Nakatsuka and Bogin before him at the time the invention was made to modify the system of Nakatsuka to include translating a virtual address into an address and caching the address and also caching another address in the same translation look aside table when the address corresponds to the translation memory space because it would have provided faster graphics data processing by allowing the operating system to provide a continuous block of AGP memory and references from the AGP memory that points to various locations in main memory to the graphics device [col. 4, lines 13-16, 24-27] as taught by Bogin.

7. Claims 8-11 and 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakatsuka et al (US6,433,782) and Bogin et al. (US6,192,455) and further in view of Hays et al (US6,356,989).

As per claims 8 and 19, the combination of Nakatsuka and Bogin discloses the claimed invention as detailed above in the previous paragraphs. However, the combination of Nakatsuka and Bogin does not specifically teach indexing a page directory based on a first portion of the virtual address to retrieve a page directory entry; indexing a page table based on the page directory and a second portion of the virtual address to retrieve a page table entry as at least part of the address as recited in the claims.

Hays discloses indexing a page directory based on a first portion of the virtual address to retrieve a page directory entry; indexing a page table based on the page directory and a second portion of the virtual address to retrieve a page table entry as at least part of the address [*portion of the linear address is utilized to index to an entry in Page Directory 104*; column 1, lines 45-58].

It would have been obvious to one of ordinary skill in the art, having the teachings of Nakatsuka and Bogin and Hays before him at the time the invention was made to modify the system of Nakatsuka and Bogin to include indexing a page directory based on a first portion of the virtual address to retrieve a page directory entry; indexing a page table based on the page directory and a second portion of the virtual address to retrieve a page table entry as at least part of the address because it would have avoided subsequent processing by the paging unit by providing starting address of the

page frame and statistical information about the page [col. 1, lines 55-57] as taught by Hays.

As per claims 9 and 20, Nakatsuka discloses determining whether the page table entry is in video graphics memory space [column 9, lines 13-22].

As per claims 10, 11, 21 and 22, Hays discloses caching and translating the page directory entry, the page table entry, and a third portion of the virtual address as the address [column 1, lines 55-58].

Allowable Subject Matter

8. Claims 1, 6, 12 and 17 are allowed over the prior art of record.

9. The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record does not teach or suggest a physical address after a first translation requires further translation and receiving a second physical page address and utilizing the second physical page address and a portion of the virtual address to produce another physical address in that both the first translation and the other second physical address are both stored in the same translation look-aside table in combination with the other elements set forth in the claimed invention.

Response to Arguments

10. Applicant's arguments filed October 17, 2003 have been fully considered but they are not persuasive. As to the remarks, applicant asserted that:

(a) The prior art of record teaches a single translation and the term "picture logical address" is equivalent to the term "logical address" with reference to the graphics processor.

Examiner respectfully traverses applicant's arguments for the following reasons. Examiner agrees with applicant that Nakatsuka discloses the term "picture logical address" is equivalent to the term "logical address" with reference to the graphics processor. However, Examiner would like to point out that Nakatsuka discloses that the "logical address" of the data processor is converted into "the picture logical address" (*or physical address*) when the data processor accesses "pixel data" as detailed in column 9, lines 5-8. Thus, when Nakatsuka discloses converting a "picture logical address" into "a physical address" to access the graphics processor (see column 9, lines 47-50), it can be seen that the "picture logical address" previously translated from the "logical address" by the data processor to access pixel data is further translated by the graphics processor to access matrix data. Note that the graphic processor 120 accesses the memory unit 200 in accordance with an instruction from the data processor 110 (see column 8, lines 50-52).

(b) The prior art of record does not teach determining whether the address corresponds to translation memory space.

Examiner respectfully traverses for the following reasons. Examiner would like to point out that Nakatsuka discloses determining whether the address corresponds to translation memory space as detailed in column 9, lines 13-22. It can be clearly seen that a determination unit is used to determine whether to translate the logical address into a physical address that belongs to a graphic region or a program region. Thus, the logical address can be converted into a tile type address if the address belongs to the graphic region or the logical address can be converted into a normal physical address if the address belongs to the program region.

(c) The prior art of record does not teach translating the address into another address when the address corresponds to translation memory space.

Examiner respectfully traverses for the following reasons. Examiner would like to point out that Nakatsuka discloses translating the address into another address when the address corresponds to translation memory space as detailed in column 9, lines 40-50. It can be clearly seen that the picture logical address [*previously converted from the logical address of the processor in step (a)*] can be further converted into a physical address to allow the graphic processor 120 to access data. Thus, two translations are required to allow the graphic processor 120 to access data. Further note that the graphic processor 120 accesses the memory unit 200 in accordance with an instruction from the data processor 110 (see column 8, lines 50-52).

(d) Bogin does not teach or suggest a process in which a virtual address is first translated into an address.

Examiner respectfully traverses for the following reasons. Examiner would like to point out that Bogin discloses translating a virtual address is first translated into an address as detailed in column 2, lines 46-49. Applicant's arguments that Bogin teaches that in the event of a non-AGP request, no address translation is needed has no relevance to applicant's claimed invention since Bogin also teaches that a virtual to main memory address translation is performed for AGP request.

(e) Bogin does not teach or suggest that the translated address is stored in a translation look aside table when the address does not correspond to the translation memory space.

Examiner respectfully traverses for the following reasons. Examiner would like to point out that Bogin discloses that the translated address is stored in a translation look aside table when the address does not correspond to the translation memory space as detailed in column 3, lines 31-39, 55-65. It can be clearly seen that address reference not within the SMRAM 134 space is stored in the GTLB 141. Note that GTLB 141 is a cache buffer of translation table 143 as detailed in column 4, lines 46-51.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre M. Vital whose telephone number is (703) 306-5839. The examiner can normally be reached on Mon-Fri, 8:30 am - 6:00 pm, alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (703) 306-2903. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Pierre M. Vital
Art Unit 2188
April 5, 2004